

# LOW COST DYNAMIC DRIVE SCHEME FOR REFLECTIVE BISTABLE CHOLESTERIC LIQUID CRYSTAL DISPLAYS

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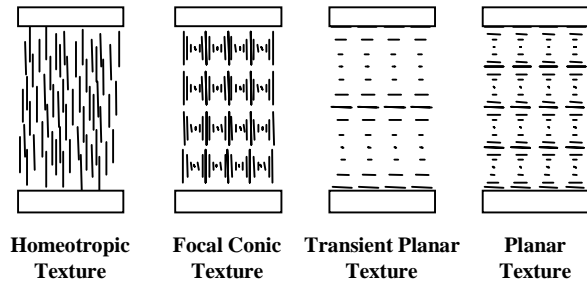
## ABSTRACT

**Bistable reflective cholesteric liquid crystal displays have significant optical and power consumption advantages over conventional liquid crystal displays. In order that they become commercially viable, their drive electronics must be inexpensive and compatible with standard information device electronics. We have developed a simplified dynamic drive scheme and the circuitry necessary to implement it using off-the-shelf components at a cost of less than \$0.03 per driver output.**

## INTRODUCTION

Bistable reflective cholesteric liquid crystal displays (ChLCDs) have many desirable optical properties which include wide viewing angles, high contrast (at least 20:1) and good performance in high ambient light conditions.

These displays make use of the different textures of cholesteric liquid crystals which are shown in Figure 1. The planar texture Bragg reflects a single wavelength of incident light, and the focal conic texture is essentially transparent.



**Figure 1.** Cholesteric liquid crystal textures.

## CHOLESTERIC TEXTURE TRANSITIONS

ChLCDs function by switching between the reflective planar texture and the transparent focal conic texture. Our drive scheme is based on first driving the ChLC into the homeotropic texture and then controlling how it relaxes to its final state. There are two mechanisms available that permit this control.

Described by Kawachi [1] in one of the first reviews of transitions in cholesteric cells, these two relaxation mechanisms are selected by the voltage that is applied to the display after the field induced homeotropic texture is achieved. The first mechanism is the nucleation induced transition from the homeotropic texture to the focal conic texture. This relaxation is possible below an applied field strength of

$$E_H = (2\sqrt{2}/\pi)E_C,$$

where  $E_C = (\pi^2/P_0)\sqrt{K_{22}/\Delta\epsilon}$  (I.S. units) was shown by DeGennes [2] to be the critical field strength necessary to unwind the cholesteric texture if the chiral axis is oriented along the plane of the cell.  $P_0$  is the intrinsic pitch of the ChLC.

The second mechanism, first pointed out by Greubel [3], is a continuous transition from the homeotropic to the planar texture via an initial conical deformation. Experimental observations revealed that this transition includes an intermediate transient planar texture that has a pitch  $P^*$  (found to be about  $2P_0$ ). Kawachi derived an expression for the field below which this second transition would take place:

$$E_{P^*} = E_H \sqrt{(P_0/2P^*)^2 - P_0/P^*},$$

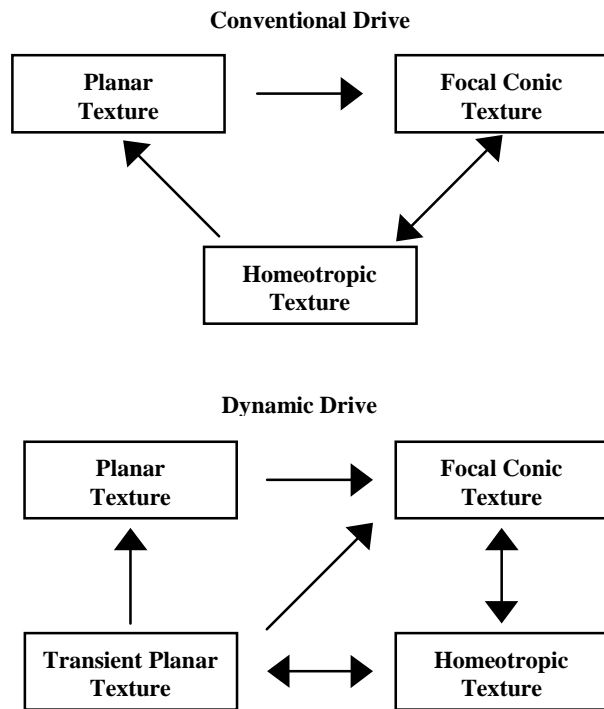
but did not explain why the conical deformation should relax to the intermediate transient planar

texture instead of directly to the equilibrium planar texture.

Yang and Palffy-Muhoray [4] Lu and Yang [5] showed by using dynamic theory that the pitch of the initial conical deformation which occurs at the start of this transition will be  $P^* = (K_{33}/K_{22})P_0$  for fields below  $E = (2/\pi)\sqrt{K_{22}/K_{33}}E_C$ .

### DRIVE SCHEMES

Two basic types of drive schemes have been developed to exploit the transitions between textures. The scheme types and the transitions they employ are outlined in Figure 2, where the arrows indicate the direction in which the transitions may proceed. Both scheme types can be described as “single page update,” suitable for displaying static text and images.



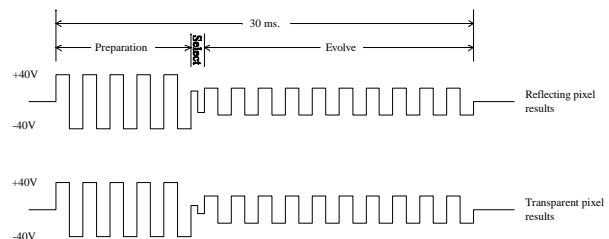
**Figure 2.** Drive schemes and the allowed texture transitions they employ.

The first scheme type utilizes three textures. It is a line at a time scheme referred to as the conventional drive. A high or low voltage is applied to a pixel in the addressed row to select the final

texture. Row write times are on the order of 5 to 10ms.

The second scheme type utilizes all four textures. Developed by Huang, Yang, Bos, and Doane [6], it is referred to as the dynamic drive scheme. Row write times of 0.5 to 1.0ms have been achieved using a pipeline algorithm. Since this algorithm permits “page turn” update rates on high resolution displays, it was selected to be adapted to low cost electronics.

The basics of the dynamic drive scheme are sketched in Figure 3. A pixel sees a voltage waveform that produces a sequence of three RMS voltages:  $V_{Preparation}$ ,  $V_{Select/Non-Select}$ , and  $V_{Evolve} \cdot V_{Preparation}$  drives the ChLC into the homeotropic regardless of its initial texture.  $V_{Select/Non-Select}$  determines if the homeotropic texture relaxes into the planar ( $V_{Select}$ ) or the focal conic ( $V_{Non-Select}$ ).  $V_{Evolve}$  serves two functions. It permits the focal conic texture to evolve from the transient planar texture that results from applying  $V_{Non-Select}$ . It also restores and maintains the homeotropic texture after  $V_{Select}$  is applied allowing relaxation to the planar texture occurs when  $V_{Evolve}$  is removed.



**Figure 3.** Original Dynamic Drive Pixel Voltage Waveforms.

Display update speed is increased by applying the common portions of each waveform,  $V_{Preparation}$  and  $V_{Evolve}$ , across many rows simultaneously. Once  $V_{Evolve}$  is removed from the last addressed row, all power is removed from the display.

### COST CONSIDERATIONS

The cost of the ChLC displays themselves has never been a concern because they are quite simple. The electrodes are patterned ITO on a glass

substrate. The ITO is overlaid with a barrier coat and an alignment layer. Spacing between substrates is  $4\mu\text{m}$  to  $5\mu\text{m}$ . Commercially available materials and standard fabrication techniques are employed throughout. No new manufacturing processes have to be developed to produce these displays.

In order to develop low cost electronics to drive these displays, we focused our attention on off-the-shelf components to take advantage of existing expertise and manufacturing capacity. We quickly settled on STN driver chips due to their voltage characteristics and their already low cost per output.

Our basic approach was to see what the STN drivers could do and then see what changes could be made to other display components to accommodate the drivers. This approach included reviewing the published specifications and learning about the unpublished ones by careful consideration of the inevitable failure modes of our prototypes. Once the failure modes were understood, systematic evaluation tests were developed so that any driver chip meeting these new performance standards could be used. These standards help make our design universal, maintaining the greatest possible independence from specific component manufacturers.

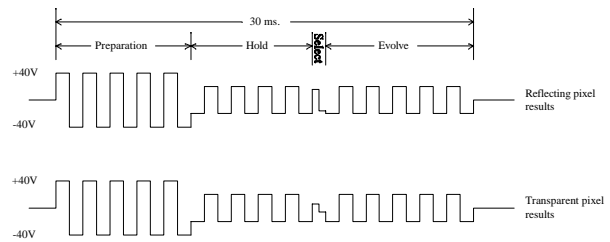
### DRIVE SCHEME MODIFICATIONS

Prior to this work, displays were typically driven into the homeotropic texture by applying a bipolar waveform ( $\sim 50V_{\text{RMS}}$ ) to a rows with high voltage electronics. Given the unipolar output voltage range of STN driver chips (nominally 0-40V), it was clear that the first change to the dynamic drive scheme would be to recast it as a differential drive scheme. The necessary large RMS voltages can only be generated across the display by the proper combination of large amplitude row and column waveforms. In addition, the displays had to be modified to lower the maximum voltage required to 40V.

The second modification arose due to a restriction of the STN-logic of the driver chips: only two of the four display voltage inputs could be applied to a display at one time by a single driver chip. The dynamic drive scheme was made

to “fit” onto the row driver chips by breaking it up into three parts and having the row driver chips function in one of three operating modes. The column driver chips also function in one of two additional operating modes.

The most significant consequence of breaking up the original dynamic drive is the addition of a new voltage to hold the ChLC in the homeotropic texture after applying  $V_{\text{Preparation}}$ . Figure 4 sketches a typical pixel waveform. Note the addition of the holding voltage before the select pulse. We will refer to this highly modified dynamic drive scheme as the Low Cost Dynamic Drive Scheme (LCDDS).



**Figure 4.** Low Cost Dynamic Drive Pixel Waveforms

The basic operation of the LCDDS is as follows. During row mode 1,  $V_{\text{Preparation}}$  is applied to the entire display. During row mode 2,  $V_{\text{Select/Non-Select}}$  is applied to the pixels in the row being addressed,  $V_{\text{Evolve}}$  is applied to those rows that have already been addressed, and a hold voltage  $V_{\text{Hold}}$  is applied to those rows not yet addressed. Chip logic dictates that  $V_{\text{Hold}}$  and  $V_{\text{Evolve}}$  must be the same and so they will be referred to as  $V_{\text{Hold/Evolve}}$ . During row mode 3, all the rows of a given row chip have been addressed, so either  $V_{\text{Hold/Evolve}}$  or a data voltage  $V_{\text{Data}}$  is applied to a row.

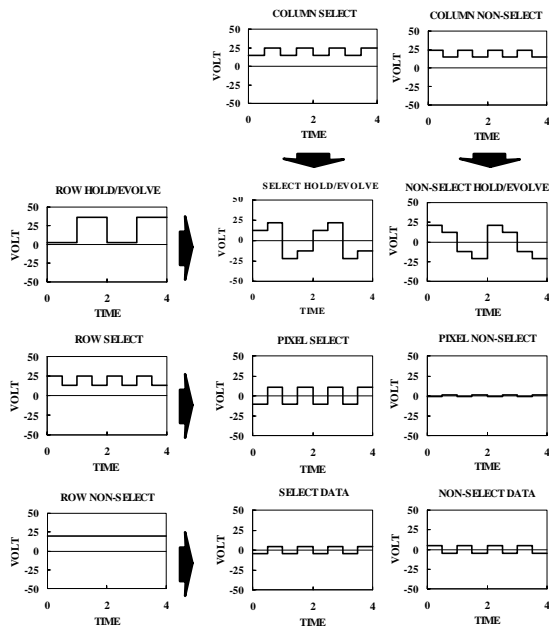
In each operating mode, the driver chips apply different waveform combinations to the display. In row mode 1, the row and column drivers apply their maximum rail voltages. In row mode two, a row driver applies either the row select waveform or the row hold/evolve waveform. In row mode 3, a row driver applies either the row hold/evolve waveform or the row non-select waveform. The

column drivers apply data waveforms to the display during row modes 2 and 3.

### LCDDS WAVEFORMS

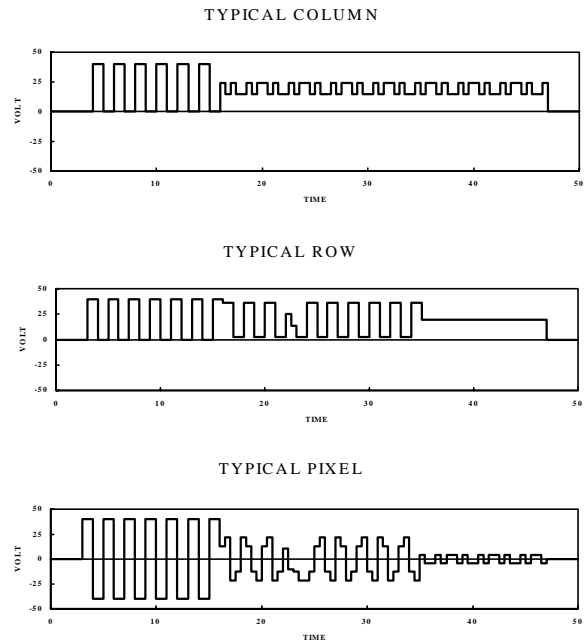
Our study of the driver chips and drive waveforms showed that lower drive voltages permit simpler drive waveforms. Simpler waveforms allow for simpler glue circuitry that supports the driver chips. We were able to lower the voltage requirements of our displays sufficiently to use the simple monopolar component waveforms of the LCDDS are diagramed in Figure 5.

The row and column preparation waveforms are simply square waves running rail to rail and are not shown. There are two column waveforms: Column Select and Column Non-Select; and three row waveforms: Row Hold/Evolve, Row Select, and Row Non-Select. Note that the RMS values of the Hold/Evolve and Data waveforms seen by the pixel are properly independent of the column waveforms.



**Figure 5.** Low Cost Dynamic Drive Component Waveforms

The component waveforms of Figure 5. are combined in Figure 6 to illustrate typical column, row, and pixel waveforms. The pixel is prepped, held, written to, evolved, and then turned off.



**Figure 6.** Low Cost Dynamic Drive Composite Waveforms

### CIRCUIT DESIGN

The block diagram for a display module implementing the LCDDS appears in Figure 7. The driver chips used on both the columns and the rows are STN column drivers with internal data latches. The latches make it possible to generate the row waveform with a minimum of additional external circuitry. The module requires as inputs seven voltage levels and two data buses for row and column data. Frame lines, clocking signals, waveform control, and the logic supply are not shown and must be supplied by an external micro-controller.

The STN column drivers generate the row waveforms in the following manner. The two intermediate voltage level inputs of the STN driver are tied together to form what we call a super-input. A row chip in the Hold/Evolve-Select mode has the row select waveform applied to its super-input by the mode select switch. The latched data then determines which state an output will be in: Hold/Evolve or Select. An output in the Hold/Evolve state swings rail-to-rail as the frame pin is toggled, thus generating the large am-

plitude Hold/Evolve portion of the waveform. An output in the Select state is mapped to the super-input, and outputs the select waveform regardless of the frame pin. The Hold/Evolve-Non-Select mode works in exactly the same way, except that the “waveform” applied to the super-input by the mode select switch is simply a DC voltage.

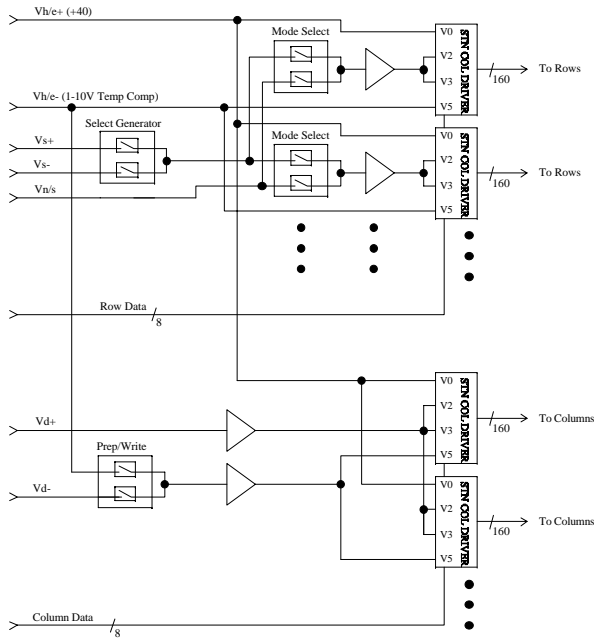


Figure 7. Display head block diagram

Compared to a typical STN drive scheme, the extra circuitry required to implement the LCDDS is minimal and low cost. As shown in Figure 7, the extra fixed circuitry in the display head consists of four analog switches (the select generator and column mode switch) and two buffer circuits. This circuitry is required regardless for the display size. The incremental circuitry needed for each row chip is shown in Figure 8. The mode select circuit analog switches and buffer circuit op amps may be non-critical commodity parts since all the required voltage swings are no greater than 20 volts.

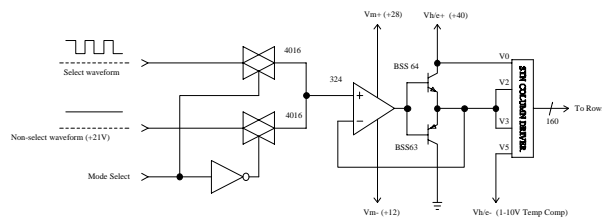


Figure 8. Incremental circuitry required for each row chip.

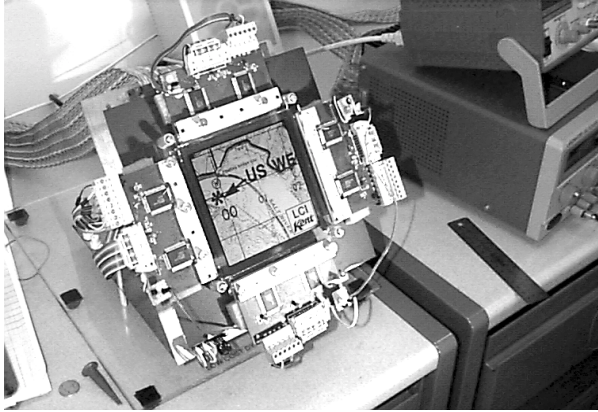
The estimated cost of row circuits for an LCDDS VGA display head is shown in Table 1 using quantity prices from typical electronics parts houses. The cost per row for the LCDDS VGA is: \$13.51/480rows = \$0.028/row. The additional cost due to the extra circuitry amounts to less than \$0.005 per row.

Row Circuit Component	Description	Cost (\$)
<b>Driver Chips</b>	3 STN column drivers, 160 outputs per driver (SED 1744 @ \$3.93 ea.)	11.79
<b>Waveform Generation</b>	2 quad bilateral switches (CD4016CM @ ¢27 ea.)	.54
<b>Buffer Circuits</b>	1 quad op amp (LM324M @ ¢34 ea)	.34
	3 npn transistors (BSS64 @ ¢14 ea)	.42
	3 pnp transistors (BSS63 @ ¢14 ea)	.42
<b>Cost for 480 rows</b>		<b>13.51</b>

Table 1. LCDDS row driver component costs.

PROTOTYPE

A prototype LCDDS display head, shown in Figure 9, has been constructed and successfully operated. A digital I/O card connects the display head to a PC. All control of the display hardware and the images occurs in software. The flexibility of this system makes it easy to optimize the LCDDS to different display configurations.



**Figure 9.** The LCDDS prototype. The display has a resolution of 80 DPI with an active area of 4" by 4".

### SUMMARY

We have developed a simple, practical, and inexpensive means of driving a bistable cholesteric liquid crystal display. Utilizing off-the-shelf components to implement our simplified low cost dynamic drive scheme, we have achieved a cost of less than \$0.03 per line.

### ACKNOWLEDGEMENTS

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### REFERENCES

- 1) M. Kawachi and O. Kogore, Jap. J. Appl. Phys. 16, 1673 (1977)
- 2) P. G. de Gennes, Solid State Com. 6, 163 (1968)
- 3) W. Greubel, Appl. Phys. Lett., 25, 5 (1974)
- 4) D.-K. Yang and P. Palffy-Muhoray, to be published.
- 5) D.-K. Yang and Z.-J. Lu, SID Digest 351 (1995)
- 6) X.-Y. Huang, D.-K. Yang, P.J. Bos., J.W. Doane SID Digest 347 (1995)